IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Nadi R. Itani et al.
Serial No.:	10/659,472
Filed:	September 10, 2003
Group Art Unit:	2622
Before the Examiner:	Hung H. Lam
Title:	Gain Control Apparatus and Method for Setting Mutually Continuous Analog, Digital, and Shutter Gain Levels

APPELLANTS' BRIEF IN SUPPORT OF APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

This brief is being submitted pursuant to 37 C.F.R. §41.37.

CERTIFICATION UNDER 37 C.F.R. § 1.10 -- FILED ELECTRONICALLY

I hereby certify that this correspondence is being deposited with the United States Postal Service as "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated below, addressed to the Mail Stop Appeal Brief – Patents, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450

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Leslie White

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I. REAL PARTY-IN-INTEREST

The real party-in-interest is Cirrus Logic, Inc., who is the assignee of the entire right and interest in the present Application.

II. RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences known to Appellants, the Appellants' legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 3 – 14 and 35 - 38 are pending in the Application.

Claims 1 – 2 and 15 - 34 are canceled.

Claims 3 – 14 and 35 - 38 stand rejected, and are the subject of the instant appeal.

IV. STATUS OF AMENDMENTS

In response to the Non-final Office Action mailed July 19, 2007, Applicants duly filed an Amendment Response to Office Action on November 15, 2007, in which selected claims were amended and arguments were presented to the Examiner to distinguish the amended claims from the cited prior art. Applicants' arguments, in light of the amended claims, were considered but not fully persuasive to the Examiner in the Final Office Action mailed March 21, 2008 (hereafter "the Final Office Action"), which prompted the present appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The principles of the present invention are generally embodied in selectable threshold multimode gain control apparatus and method for setting mutually continuous analog, digital, and shutter gain levels. By utilizing such selectable threshold multimode gain control apparatuses and methods, gain is able to be separately controlled over analog and digital subsystems. Advantageously, the present invention provides integrated gain control effective for both the analog as well as the digital portions of a combined camera system.

Independent Claim 3 defines an embodiment of a distributed gain control circuit (DGCC) *(Application, Figures 2 and 3, digital gain circuit 117, and page 8, lines 15 to 20)*. The DGCC has an imager signal source that includes a shutter (*Application, Figure 3, imager signal IMAGE, shutter speed, SHUTTER, page 9, lines 7 to 14*). A timing circuit controls the shutter and the production of signals from said imager signal source (*Application, Figure 3, Timing Block Circuit 181, page 10, lines 12 to 21*) , . A CDS/VGA system receives imager signals from the imager signal source (*Application, Figure 3, Correlated Double Sample/Variable Gain Amplifier (CDS/VGS) circuit 114, page 9, lines 17 to 24)*. An analog to digital converter connected to the CDS/VGA system receives an amplified imager signal stream from said CDS/VGA system and converts the amplified imager signal stream into digital form, and digital gain circuit is connected to the analog to digital converter (*Application, Figure 3, ADC 116, Digital Gain Circuit 117,*

page 9, line 17 to page 10, line 3). An automatic gain control (AGC) circuit has a gain splitter circuit for receiving gain values which the digital gain circuit has determined, and the gain splitter circuit produces distributed gain values from the received gain values (*Application, Figures 3 and 5B, 5C, and 5D, Figures 9A to 9D, AGC 119, first splitter 197, second splitter 198, received gain values, shutter gain value, chip gain values, digital gain code value and analog gain code value, ...distribute gain, page 9, line 24 to page 10, line 3, page 12, line 29 to page 15, line 28, page 18, line 26 to page 19, line 3).*

Dependent Claim 4 further defines that the AGC circuit is coupled to said timing circuit for controlling the production of signals from said imager signal source (*Application, Figures 3 and 4, AGC 119, timing block circuit 181, page 9, line 24 to page 11, line 17).*

Independent Claim 5 defines a method of gain control in an imaging system having a shutter (*Application, Figure 3, imager signal IMAGE, shutter speed, SHUTTER, page 9, lines 7 to 14*), a digital gain circuit *(Application, Figures 2 and 3, digital gain circuit 117, and page 8, lines 15 to 20)* and a CDS/VGA circuit (*Application, Figure 3, Correlated Double Sample/Variable Gain Amplifier (CDS/VGS) circuit 114, page 9, lines 17 to 24).* The method of gain control involves determining a total gain for an imaging system (*Application, Figure 3, total gain range of the chip and shutter, page 9, line 30 to page 10, line 3*). The method involves receiving, by an automatic gain control (AGC) circuit having a gain splitter circuit, the determined total gain, and the

method also involves splitting, by the gain splitter circuit, the determined total gain into distributed gain values which at least include a shutter gain, an analog (VGA) gain, and a digital gain (*Application, Figures 3 and 5B, 5C, and 5D, AGC 119, first splitter 197, second splitter 198, received gain values, shutter gain value, chip gain values, digital gain code value and analog gain code value, page 9, line 24 to page 10, line 3, page 12, line 29 to page 15, line 28).* The method additionally involves determining the level of the shutter gain to be applied in the operation of the imaging system; determining the level of the analog (VGA) gain to be applied in the operation of the imaging system; and determining the level of the digital gain to be applied in the operation of the imaging system(*Application, Figures 3 and 5B, 5C, and 5D, AGC 119, first splitter 197, second splitter 198, received gain values, shutter gain value, chip gain values, digital gain code value and analog gain code value, page 9, line 24 to page 10, line 3, page 12, line 29 to page 15, line 28).*

Dependent Claim 6 further defines that each gain setting for said imaging system is applied for the duration of a single frame (*Application, Figure 5A, ...AGC value to be incremented, decremented, or left unchanged for each frame, page 12, lines 14 to 17).* Dependent Claim 7 further adds that shutter gain, the analog (VGA) gain, and the digital gain are hierarchically adjusted (*Application, Figure 4, shutter gain, chip gain applied through CDS/VGA circuit 114, and digital 117, page 10, line 31 to page 11, line 5*). Dependent Claim 8, which depends from Claim 7, further defines that the shutter gain has maximum and minimum shutter gain values (*Application, Figure 5C, maximum and*

minimum shutter gains, page 13, line 15 to page 14, line 15). Dependent Claim 9, which depends from Claim 7, further defines that the analog (VGA) gain has maximum and minimum analog gain values (*Application, Figure 5D, maximum and minimum VGA gains, page 14, line 25 to page 15, line 28*). Dependent Claim 10 further defines that a chip gain has a maximum and a minimum gain value (*Application, Figure 5C, maximum and minimum chip values, page 13, lines 11 to 13*). Dependent Claim 11 further defines that the digital gain has a maximum and a minimum value (*Application, Figure 5D, maximum and minimum digital gains, page 14, line 28 to page 15, line 28*).

Dependent Claim 12 further defines that the analog (VGA) gain and the digital gain remain at a constant level as the shutter gain is varied (*Application, Figures 5A to 5D, ...AGC value to be incremented, decremented, or left unchanged for each frame, page 12, lines 14 to 17, and page 11, line 18 to page 15, line 28)*. Dependent Claim 13 further defines that the shutter gain and the analog (VGA) gain remain at a constant level as the digital gain is varied (*Application, Figures 5A to 5D, ...AGC value to be incremented, decremented, or left unchanged for each frame, page 12, lines 14 to 17, and page 11, line 18 to page 15, line 28)*. Dependent Claims 14 further defines that the shutter gain and the digital gain remain at a constant level as the analog (VGA) gain is varied (*Application, Figures 5A to 5D, ...AGC value to be incremented, decremented, or left unchanged for each frame, page 12, lines 14 to 17, and page 11, line 18 to page 15, line 28)*. Dependent Claims 35, 36, and 37 further define for respective Claims 12, 13, and 14 that the constant level is user-settable (*Application, Figures 5C and 5D,*

"...programmable or user settable values.", page 14, lines 2 to 5, page 15, lines 11 to 15). Dependent Claim 38, which depends from Claim 3, further defines the distributed gain values are split into shutter gain values, analog gain values, and digital gain values (*Application, Figure 5B, input received gain values, shutter gain values, chip gain values, digital gain code value, analog (VGA) gain code value, ...distribute gain, page 12, line 29 to page 13, line 7, page 18, line 26 to page 19, line 3*).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) Are Claims 3 to 12, 14, and 38 properly rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,982,424 to Simerly (hereafter "the *Simerly* reference")?

(B) Are Claims 13 and 35 to 37 properly rejected under 35 U.S.C. § 103(a) as being unpatentable as over the *Simerly* reference in view of U.S. Patent No. 5,657,077 to DeAngelis (hereafter "the *DeAngelis* reference")?

VII. ARGUMENT

(A) Points and Authorities

Anticipation rejections under 35 U.S.C. § 102(e) require identity of invention. In other words, each and every feature of each and every claim rejected as anticipated must be shown in a single prior art reference. *Tyler Refrigeration v. Kysor Indust. Corp.*, 777 F.2d 687, 227 USPQ 845 (Fed. Cir. 1985); *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989); *Glaverbel S.A. v. Northlake Mkt'g & Supp., Inc.*, 45 F.3d 1550, 33 USPQ2d 1496 (Fed. Cir. 1995) (The claimed invention, as described by properly construed claims, must be the same as that of the reference). Furthermore, to anticipate, a reference must be enabling in order to place the allegedly disclosed matter in the possession of the public. In other words, the reference must describe the applicant's claimed invention sufficiently to have placed a person of ordinary skill in the field of the invention in possession of it. *Akzo N.V. v. United States ITC*, 808 F.2d 1471, 1 USPQ2d 1241 (Fed. Cir. 1986); *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990).

All analyses of nonobviouness under 35 U.S.C. §103 begin with the well-established objective guidelines set forth in *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17 – 18 (1966):

> "Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviouness or nonobviousness of the subject matter is determined."

Application of the *Graham* guidelines requires that a flexible and expansive approach be taken when determining obviousness. *KSR International Co. v. Teleflex Inc. Et Al., 550 U.S. __, ___, 127 S. Ct. 1727, 1739 (2007).* To this end, the obviousness analysis cannot be confined by a formulistic conception of the words teaching, suggestion, and motivation, or by the overemphasis on the importance of published articles and the explicit content of issued patents. *127 S. Ct. at 1741.*

Nevertheless, the Court in *KSR* recognized that more is required for a finding of obviousness than a mere identification in the prior art of all the elements of a claimed combination of elements:

> "As is clear from cases such as *Adams,* a patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art. Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." Id, at 127 S. Ct. at 1741, citing *United States v. Adams,* 383 U.S. 39 (1966).

The Federal Circuit has similarly recognized that there are no all-purpose criteria for applying the law of obviousness to every factual situation; all relevant facts must be considered, while recognizing that it is inappropriate to squeeze new factual situations into pre-established pigeonholes. *In re Eli Lilly & Co.*, 902 F.2d 943 (Fed. Cir. 1990). The totality of the evidence must be considered to avoid the hindsight syndrome wherein that which only the inventor taught is used against its teacher. *In re Corkill*, 771 F.2d 1496 (Fed. Cir. 1985). Moreover, the prior art must be evaluated as a whole, since the test for obviousness is what the combined teachings of the references would have suggested to one skilled in the art. *In re Young*, 927 F.2d 588 (Fed. Cir. 1991).

(B) The Rejections of Claims 3 to 12, 14, and 38 under 35 U.S.C. § 102(e) as being anticipated by the *Simerly* reference.

In the Final Office Action, the examiner believes that "the broadest interpretation of the present claimed invention does in fact read on the cited reference for at least the reasons discussed above and as stated in the detail Office Action...". However, Applicants' disagree with the examiner's read of the *Simerly* reference on applicants' claims. Contrary to the examiner's assertion made in the Final Office action that in independent Claims 3 and 5 an automatic gain control circuit (AGC) receiving the determined gain or determined gain values and the AGC having a gain splitter circuit that produces from or splits the determined gain or determined gain values into distributed gain values are taught or disclosed, the *Simerly* reference does not in any way teach or disclose such features. Applicants have examined in detail the specific

citations in the Final Office Action that the examiner has made with respect to rejecting independent Claims 3 and 5. Applicants cannot find anywhere in the *Simerly* reference the teaching or disclosure of determined gain/determined gain values and a gain splitter circuit that produces from/splits the determined gain/determined gain values into distributed gain values. Thus, the examiner's anticipation rejections of independent Claims 3 and 5 cannot stand, and independent Claims 3 and 5 are allowable for these reasons. Also, Claims 4, 6 to 12, 14, and 38 are dependent claims from respective Claims 3 and 5, and they are allowable for at least the same reasons that Claims 3 and 5 are allowable.

Furthermore, with respect to Claim 7, the examiner admits in the Final Office Action that he relies on inherency for rejecting this claim, and the fact is that the *Simerly* reference does not in any way explicitly teach or disclose hierarchically adjusting the shutter gain, the analog (VGA) gain, and the digital gain. Thus, Claim 7 is not anticipated by the *Simerly* reference for this further reason. Additionally, with respect to Claim 8, the examiner admits in the Final Office Action that he relies on inherency for rejecting this claim, and the fact is that the *Simerly* reference does not in any way explicitly teach or disclose the shutter gain having maximum and minimum shutter gain values. Thus, Claim 8 is not anticipated by the *Simerly* reference for this further reason. With respect to Claim 9, the fact is that the *Simerly* reference does not in any way explicitly teach or disclose the analog (VGA) gain having maximum and minimum analog gain values. Thus, Claim 9 is not anticipated by the *Simerly* reference for this

further reason. With respect to Claim 10, the fact is that the *Simerly* reference does not in any way explicitly teach or disclose a chip gain having a maximum and a minimum gain value. Thus, Claim 10 is not anticipated by the *Simerly* reference for this further reason. With respect to Claim 11, the fact is that the *Simerly* reference does not in any way explicitly teach or disclose the digital gain having a maximum value and a minimum value. Thus, Claim 11 is not anticipated by the *Simerly* reference for this further reason.

With respect to Claim 12, the examiner admits in the Final Office Action that he relies on inherency for rejecting this claim. Contrary to the examiner's assertion, the fact is that the *Simerly* reference does not in any way teach or disclose the analog (VGA) gain and the digital gain remaining at a constant level as the shutter gain is varied. Again, applicants have examined the *Simerly* reference in detail and cannot find such a recitation of this feature. Thus, Claim 12 is not anticipated by the *Simerly* reference for this further reason. Additionally, with respect to Claim 14, the examiner admits in the Final Office Action that he relies on inherency for rejecting this claim. Contrary to the examiner's assertion, the fact is that the *Simerly* reference does not in any way teach or disclose the shutter gain and the digital gain remaining at a constant level as the analog (VGA) gain is varied. Applicants have examined the *Simerly* reference in detail and cannot find such a recitation of this feature. Thus, Claim 14 is not anticipated by the *Simerly* reference for this further reason. With respect to Claim 38, the *Simerly* reference does not in any way teach or disclose the distributed gain values are split into shutter gain values, analog gain values, and digital gain values.

Applicants have examined the *Simerly* reference in detail and cannot find such a recitation of this feature. Thus, Claim 38 is not anticipated by the *Simerly* reference for this further reason.

Therefore, for the above reasons, the examiner's anticipation rejections of Claims 3 to 12, 14, and 38 cannot stand, and Claims 3 to 12, 14, and 38 are clearly allowable over the cited prior art.

(C) The Rejections of Claims 13 and 35 to 37 under 35 U.S.C. § 103(a) as being unpatentable over the *Simerly* reference in view of the *DeAngelis* reference.

Claim 13 is dependent from Claim 8. Claim 35 is dependent from Claim 12. Claim 36 is dependent from Claim 13, and Claim 37 is dependent from Claim 14. Thus, Claims 13 and 35 to 37 are distinguished from the *Simerly* reference based on the same reasons that Claims 8, 12, and 14 are distinguished from the *Simerly* reference as stated above.

The examiner admits that he relies on inherency for rejecting Claim 13 in that he concludes that the *Simerly* reference inherently teaches the shutter gain and the analog (VGA) gain remain at a constant level. Applicants have examined the *Simerly* reference in detail and cannot find such a recitation of this feature. The examiner further cites the *DeAngelis* reference in rejecting Claims 13 and 35 to 37. However, the *DeAngelis* reference also does not cure the deficiencies of the *Simerly* reference. For example,

with respect to Claim 13, the *DeAngelis* reference does not in any way teach or suggest the shutter gain and the analog (VGA) gain remaining at a constant level as the digital gain is varied. Also, with respect to Claims 35 to 37, the DeAngelis reference does not explicitly teach or suggest the constant level being user settable.

Thus, the *Simerly* reference and/or the *DeAngelis* reference, either taken alone or in combination, do not teach or suggest the shutter gain and the analog (VGA) gain remaining at a constant level as the digital gain is varied and also do not teach or suggest the constant level being user settable. Therefore, for the above reasons, the examiner's obviousness rejections of Claims 13 and 35 to 37 cannot stand, and Claims 13 and 35 to 37 are clearly allowable over the cited prior art.

(D) Conclusion

Reversal of the rejections and allowance of the Application is respectfully requested.

Respectfully submitted,

Cirrus Logic, Inc.

By: /STEVEN LIN/
Steven Lin
Reg. No. 35,250

2901 Via Fortuna
Austin, Texas 78746
(512) 851-4465
Date: 21 OCTOBER 2008

VIII. CLAIMS APPENDIX

1. (Cancelled)

2. (Cancelled)

3. A distributed gain control circuit (DGCC) comprising:

an imager signal source including a shutter;

a timing circuit for controlling said shutter and

the production of signals from said imager signal source;

a CDS/VGA system for receiving imager signals from said imager signal source;

an analog to digital converter connected to said CDS/VGA system for receiving an amplified imager signal stream from said CDS/VGA system and converting the amplified imager signal stream into digital form;

a digital gain circuit connected to said analog to digital converter; and

an automatic gain control (AGC) circuit having a gain splitter circuit for receiving gain values which the digital gain circuit have determined and wherein the gain splitter circuit produces distributed gain values from the received gain values.

4. The DGCC according to claim 3 wherein said AGC circuit is coupled to said timing circuit for controlling the production of signals from said imager signal source.

5. A method of gain control in an imaging system having a shutter, a digital gain circuit, and a CDS/VGA circuit, including:

determining a total gain for an imaging system;

receiving, by an automatic gain control (AGC) circuit having a gain splitter circuit, the determined total gain;

splitting, by the gain splitter circuit, the determined total gain into distributed gain values which at least include a shutter gain, an analog (VGA) gain, and a digital gain; and

determining the level of the shutter gain to be applied in the operation of the imaging system;

determining the level of the analog (VGA) gain to be applied in the operation of the imaging system; and

determining the level of the digital gain to be applied in the operation of the imaging system.

6. The method according to claim 5, wherein each gain setting for said imaging system is applied for the duration of a single frame.

7. The method according to claim 5 including hierarchically adjusting the shutter gain, the analog (VGA) gain, and the digital gain.

8. The method according to claim 7 wherein the shutter gain has maximum and minimum shutter gain values.

9. The method according to claim 7 wherein the analog (VGA) gain has maximum and minimum analog gain values.

10. The method according to claim 7 wherein a chip gain has a maximum and a minimum gain value.

11. The method according to claim 7 wherein the digital gain has a maximum and a minimum value.

12. The method according to claim 8 wherein the analog (VGA) gain and the digital gain remain at a constant level as the shutter gain is varied.

13. The method according to claim 8 wherein the shutter gain and the analog (VGA) gain remain at a constant level as the digital gain is varied.

14. The method according to claim 8 wherein the shutter gain and the digital gain remain at a constant level as the analog (VGA) gain is varied.

Claims 15 through 34 (Cancelled).

35. The method according to claim 12, wherein said constant level is user-settable.

36. The method according to claim 13, wherein said constant level is user-settable.

37. The method according to claim 14, wherein said constant level is user-settable.

38. The DGCC according to claim 3 wherein the distributed gain values are split into shutter gain values, analog gain values, and digital gain values.

IX. EVIDENCE APPENDIX

None

X. RELATED PROCEEDINGS APPENDIX

None